Indian Journal of Research Communication Engineering (IJRCE)
Vol.3.No.1 2015 pp 1-8
available at: www.goniv.com
Paper Received :20-03-2015
Paper Published:14-04-2015
Paper Reviewed by: 1. Dr.A.Subashree 2. G.Rajbharath
Editor : Prof. P.Muthukumar

Interleaving Test Algorithm for Subthreshold Leakage-Current Defects in DRAM

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Abstract

Dynamic RAM cell is a continuous improvement in various technology and has been down-scaled, several studies have been carried out to determine ways to protect cell data in the minimum feature size dynamic ram from leakage current in many areas. In the field of testing more appropriate test algorithms are required to detect weak cells with leakage current sources. The project propose an interleaving test algorithm that takes into account the equal bit-line stress regardless of the cell location. The proposed test algorithm allows screening of weak cells that cannot hold cell data due to the subthreshold leakage current. During the stress period the algorithm can also detect other leakage currents. The project presents the maximum stress differences according to the cell location and determines the influence of the refresh operation on the maximum stress time.

Key words— Bit-line stress time, maximum stress time,subthreshold leakage-current defect, test algorithm.

I.INTRODUCTION

The simple structure of the dynamic RAM (DRAM) cell and continuous improve-ment in lithography and dry-etching technology has made DRAM grow exponentially in a large-scale integration and has decreased the minimum feature size in memory chips [1]. Forbetterperformance and lower power consumption, the memory chip has been scaled down every year. The 2010 ITRS roadmap reports that the minimum feature size of DRAM will be 20 nm in 2017 and 10 nm in 2023 [2]. However, with this down-scaling trend of the minimum feature size and power, many problems (capacitor/word line/bit-line bridges, coupling noise, P-MOS/N-MOS ratio, leakage current, and so on) need to be considered. Furthermore, due to the demands of higher density and speed, the leakage-current problem.The propose an interleaving test algorithm that takes into equal bit line stress regardless of the cell location. The proposed test algorithm for screening the weak cells that cannot hold the cell data due to the subthershold leakage current during the stress

period the algorithm can also detect other leakage current. With the short length of the word-line channel, the subthreshold leakage current will increase more .To prevent this subthreshold leakage-current problem, channel doping should be increased in order to maintain adequate control of short-channel effects.

However, junction leakage current due to band-to-band tunneling and gate-induced drain leakage current may increase as a result of high channel doping.The architecture for an the proposed algorithm, an interleaving test for to detect leakage current in the cell data. The test algorithm for check the data in row and column based arrange sequentially. The test algorithm for reduce the time delay and activate cell of refresh.The scrambling process for an test algorithm implement data back round row and column direction. The data are written into the cells connected to the bit bar line to identify the weak cell data .

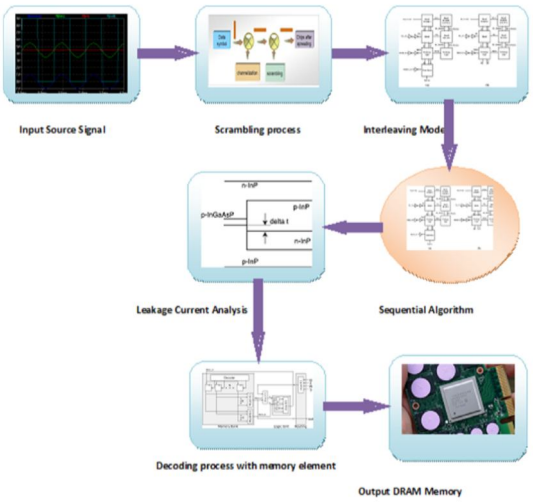

Fig.1:Blockdiagramfor dynamic ram

The screening technique using detect the weak cell data the sequential algorithm or serial algorithm is an algorithm that is executed sequentially.The term is primarily used to contrast with algorithm serial or parallel algorithm. If these need to distinguished, the opposing sequential/concurrent and serial/parallel may be used.The ternary framework contains a larger set of binary. Present a taxonomy that embeds all binary and ternary decoding strategies that the zero symbol of biases that require redefinition of the decoding design. The paper proposes a new efficient test algorithm for equal bit-line stress in order to screen for subthreshold leakage-current defects. During the stress time, the algorithm can detect other leakage-current defects. First, the leakage-current sources and scrambling technique are discussed, and then the proposed test algorithm operation is explained. The influence of the refresh operation is investigated, and the stress time of the proposed test algorithm is simulated taking into account DRAM refresh. In terms of equal bit-line stress, a correlation between the refresh and read time is suggested. Finally, the test results are discussed to demonstrate the performance of the new test algorithm.

2.EXISTING SYSTEM

The previous algorithm for binary algorithm used this for an increasing the subthershold leakage current /word line/bit-line bridges, coupling noise, P-MOS/N-MOS ratio), leakage current.High power consumption ,low density and memory defect .Due to the demands of higher density and speed, the leakage-current problem has recently become more serious. Many problems (capacitor serious. With the short length of the word-line channel, the subthreshold leakage current will increase more. To prevent this subthreshold leakage-current problem, channel doping should be increased in order to maintain adequate control of short-channel effects.

3.RELATED WORK

Recent years research efforts have been made for leakage energy reduction techniques. Muk *et al*leakage current mechanism and leakage reduction.

Cin et al optimization of burn in test adaptive process .Bhat et al making dram refresh. Hao et al Fault in dram process. Kas et al reducing the high voltage in stress test.

the two dominant leakage paths (V to round and bitline to ground) for a six-transistor DRAM cell. Leakage through these two paths consist a high percentage

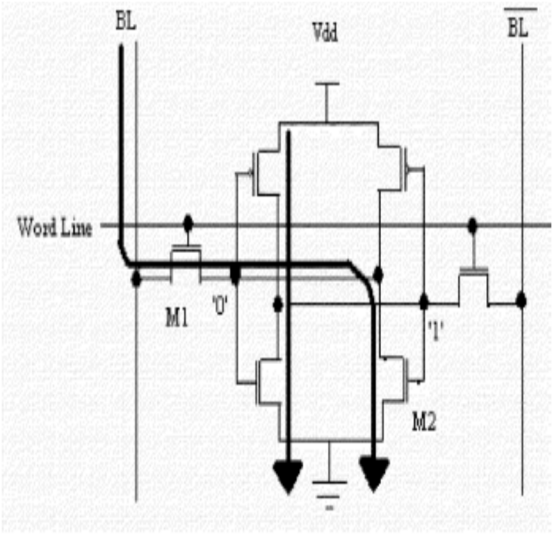

Fig.2: Schematic of a dynamic RAM

cache line to a high state right after its access, leavesthe cache line in low for a certain period (30–100 s).The ensures that the upcoming accesses within this period will not impose any energy or delay penalties. Moreover ,using the spatial locality of program reference, instead of only turning on the accessed cache line, a portion of the cache containing the accessed cache line is turned on. Consequently, subsequent accesses occur in the turned-on portion of the cache. A capacitor-discharging scheme is described in to implement the body-bias control circuit.

ALGORITHM

Interleaving test algorithm for new efficient test algorithm for equal bit-line.Refresh operation is investigated,and the stress time of the proposed test algorithm is simulated taking into account DRAM refresh.

4.INTERLEAVING TEST ALGORITHM

Data scrambling means that logically adjacent data are not physically adjacent. Fig. 3 shows the twisted address line between the physical and logical addresses and the data status when the value of 0 is transferred to the cells without using scrambling scheme. In this case, the logical address ofWL4, 5, 6, and 7 is different from the physical address due to the efficiency of the memory layout. And in case of the memory cell, which is based on the bit line, the inverted data are written into the cells connected to the bit bar line.

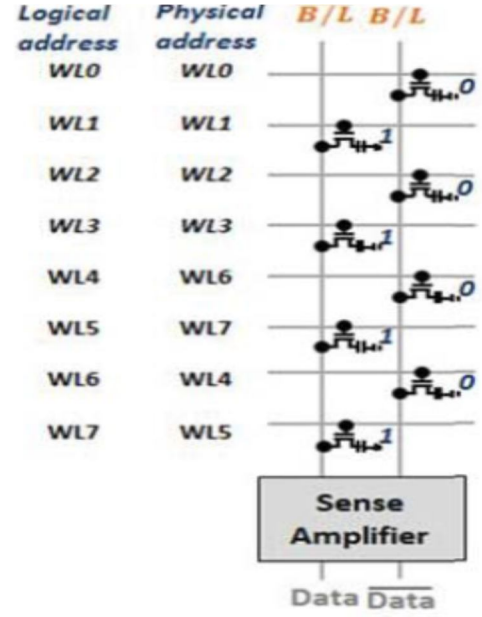

Fig.3:Address and data scrambler

The concept of the proposed test algorithm for DRAM array is composed of eight rows and

one column, and is implemented using a 2-Row Bar data background with scrambling enabled. Cells of word lines0, 1, 4, and 5 are stored as “0,” and cells of word lines2, 3,6, and 7 are stored as “1.” During the read operation of the first word line, the data stored as “0” is transferred to the bitWhen the first word line is activated at a specified time, thebit-line cells stored as “1” arestressed during the activated

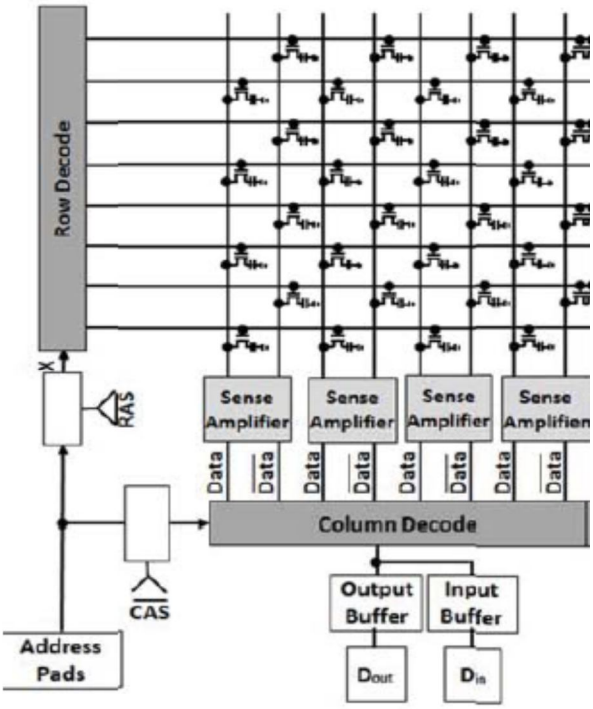

Fig.4:Row Bar data background

certain number of times, then the cells stored as opposite with the bit line and bit bar line are stressed during the activated time. If cells have a defect caused by the threshold leakage-current data, the defect-cell data are easily changed to the opposite value during the stress time. Furthermore, these defects can be detected by setting an appropriate activated time of the word line depending on screenability .the test algorithm in (2) is applied using a solid databackground with data scrambling cell i is on the even word line and is connected to the bit line. By the operation of (wa), all cells are written as “0.” When the read operation of even cells is performed, the bit line is charged to “0” due to the activated cell data. Thus, cell i is not stressed cell data of I activated.

1.LEAKAGE REDUCTION TECHNIQUES

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power dueto charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage current through each transistor.

A.Channel for leakage reduction

Based on constant field scaling the SCE can be keptunder control by scaling down the vertical dimensions, for example, gate insulator thickness, junction depth, along with the horizontal dimensions, while also proportionally decreasing the applied voltages. The substrate doping concentrationshould increase to decrease the depletion width proportionally. This is shown schematically .The principle of constant field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, such that the electricfield remains unchanged. Constant electric field assures the reliability of the scaled device in terms of hot-carrier injection a key parameter is the maximum gate depletion width,, within which mobile carriers (holes in the case of nMOSFETs) are swept away by the applied gate field.

B.Circuit for leakage reduction

Due to the positive source potential ,gate-to-source voltage of becomes negative; hence, the subthreshold current reduces substantially. Due to , body-to-source potential of becomes negative, resulting in an increase in the threshold voltage (larger body effect) of , and thus reducing the subthreshold leakage. Due to , the drain to source potential of decreases, resulting in an increase in the threshold.

C.Decoding

The design of the decoding cores must yield the same degree of flexibility of the being us independent as possible of the set of supported codes.decoding for serial ldpc decoding.

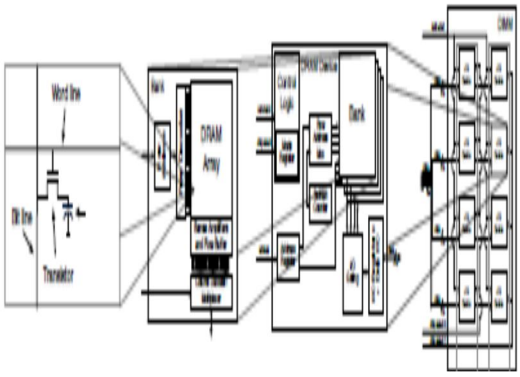

Fig.5:Memory module of DRAM

Memory organization evolves from the idea presented which in every decoding core two memories instantiated7-bit memory and a 5-bit memory. Their usage is shown in the left part of LDPC VN-to-CN values are stored in the 7-bit memory, together with turbo extrinsic information and state metrics. The 5-bit memory is instead used for CN-to-VN values in LDPC decoding, while storing the intrinsic channel information in turbo decoding. The memories are sized to the largest WiMAX codes for LDPC and for turbo).

However, according to post-layout synthesis results, memory access multiplexers suffer from excessive area overhead for these particular cuts.

To reduce this problem and to reduce at the same time .

D.Memory Scheduling:

Both 6-bit and 2-bit memories areimplemented as dual port RAMs, allowing two concurrent operations.

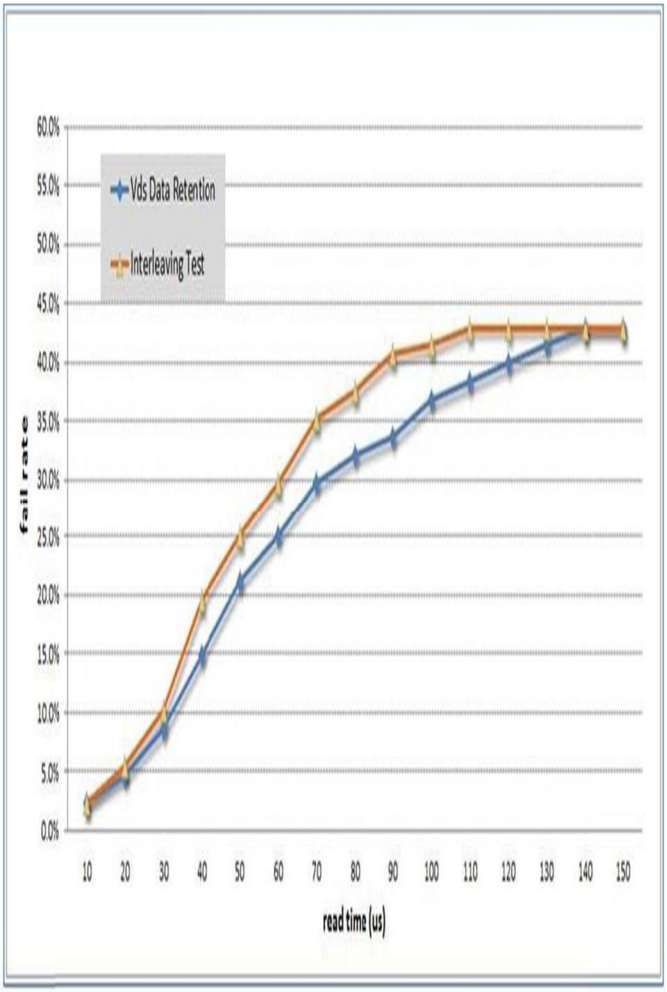

Fig.6:coverage of read time

4. EXPERIMENTAL SETUP

The MSTi results for the interleaving model are listed in cells on the bit line are stressed only when cells on bit bar lines are activated. Thus regardless of the cell location cells on the bit line or bit bar line have stress times that are half of the word line length.The MSTi of the interleaving mode has fixed values that differ according to the data back round and scrambling conditions regardless of the location of cell these results overcome the variation in stress according to the cell locations however,if the refresh operation is applied to the interleavingtest results stress initialization performed due to the refresh to verify this analysis Experiments were conducted with 2G bit DRAM chips.As the bit line stress is analyzed theoretically in Section III, the bit line stress differ depending on the scrambling and data back round. Line stress differs depending on the scrambling and data background. among the combinations of data background and scramble, the screencoverage was greatest with the combination of a solid data background and scrambling enabled, as mentioned previously in the discussion of the MSTi of cells. Therefore, in experiment, we used a solid data background with scrambling enabled. And the test is carried out by setting the refresh condition based on the W/L size in order to optimize the maximum stress time In the experiments demonstrated that the screen, it is necessary to confirm adequate read time in order to screen the subthreshold leakage-current coverage varies according to the read time, so the screenability increases as the read time increases.

5.Results of the Design Flow:By performing the interleaving test algorithm following the proposed design flow the leakage current reduction in memory element efficient increseas storage the data.

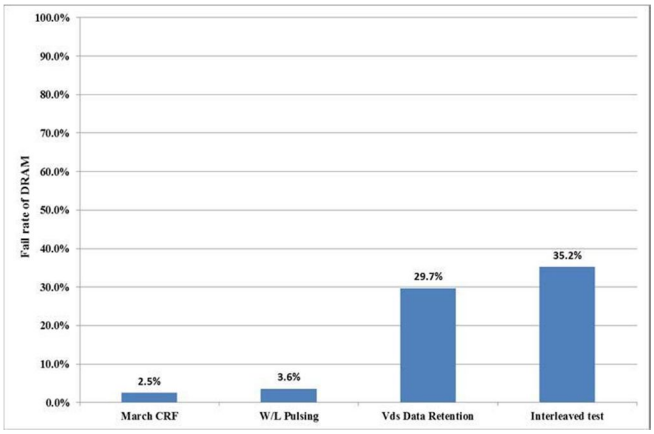

Fig.7:Screen coverage

RESULT

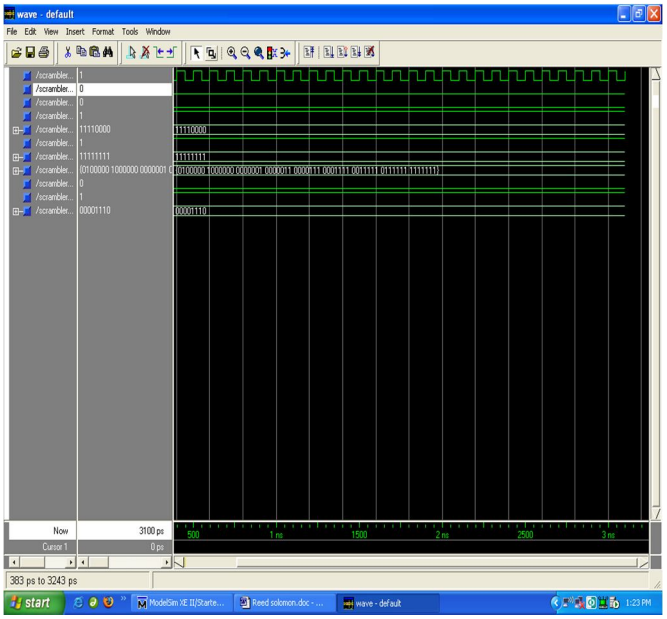

Fig.8:Input signal

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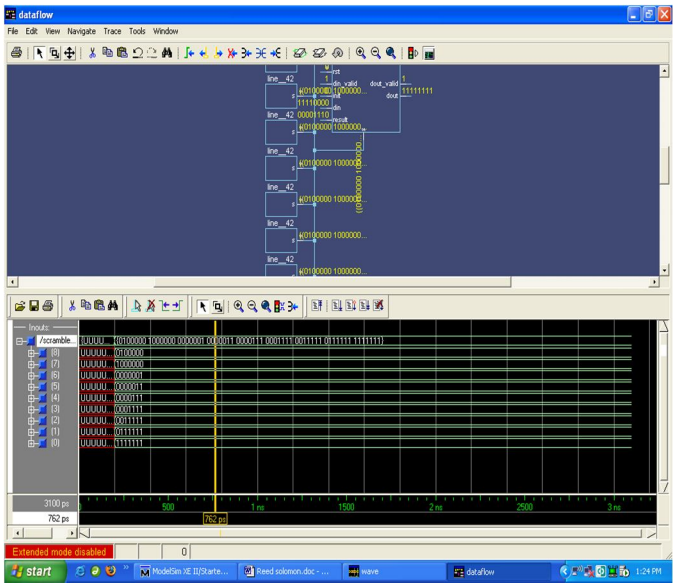

Fig.9:Data flow

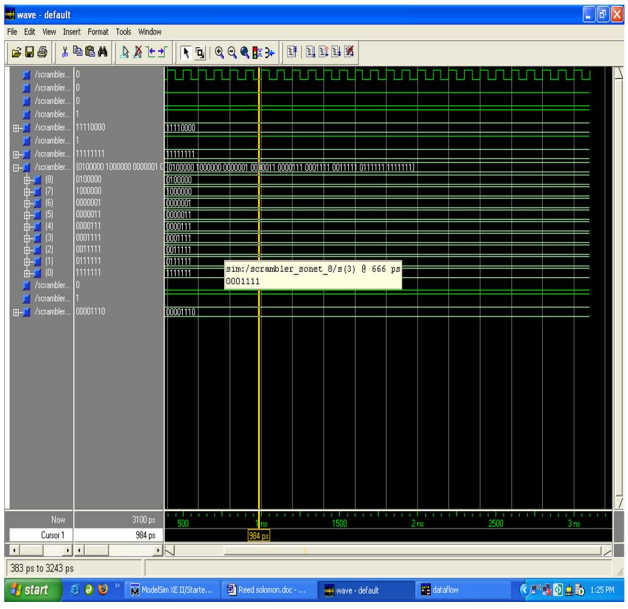

Fig.10 Scrambling Process

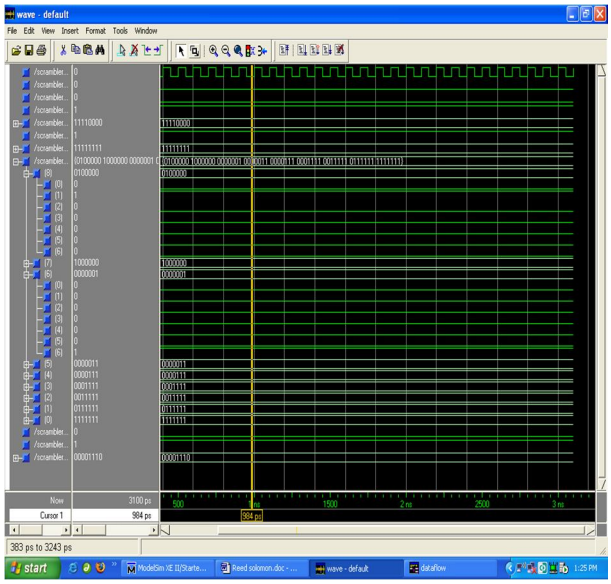

Fig.11 Output signal

CONCLUSION

DRAM, subthreshold leakage-current faults have become more serious in the MST according to cell location and to determine the optimized refresh conditions, simulations are conducted under various test condition. Therefore, the paper proposes a new test algorithm to detect subthreshold leakage-current faults. The screenability and efficiency are experimentally compared between the previous test algorithm and the proposed test algorithm. As a result of the experiment, the proposed test algorithm has a higher screenability of about 6% and reduces test time by about 20% compared with the previous test algorithm. Test conditions of the test algorithm can differ depending on the DRAM cell array and design, but proper test conditions and flexibility can be by adjusting the read time and refresh cycle. The proposed test algorithm

can be used not only to reduce thetest time, but also to improve device quality.

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